Rambus Signal Quality Measurements

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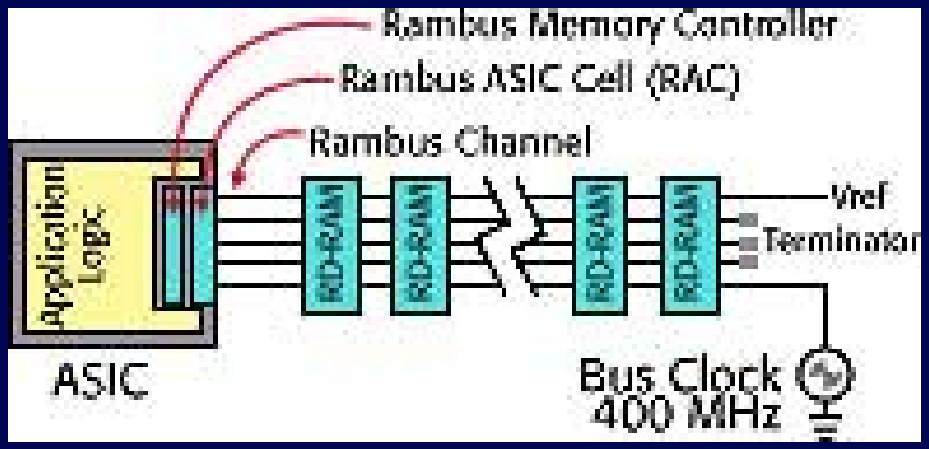
Rambus Signal Quality Challenges



- High Speed Bus
- Stringent Timing Requirements
- Fast Signal Edges
- Low Jitter Signals
- Pipeline Architecture

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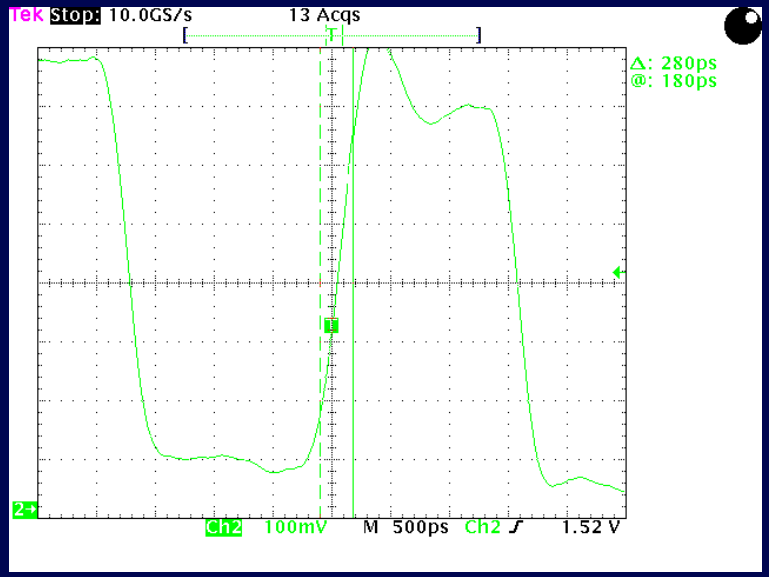
Rambus Technology Rise/Fall Time Requirements

Page 34, Direct RAC Data Sheet:

Rambus T_r and T_f = 200ps

Source: www.rambus.com



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Rambus Rise/Fall Time Instrumentation Requirements

- 200ps RT Oscilloscope has BW = 0.35/T = 1.75GHz
- RT(measured) = SQRT[RT(oscilloscope)^2 + RT(probe)^2 + RT(Signal)^2]
- RT (measured) = SQRT[200ps^2 + 200ps^2 + 200ps^2] = 346ps!
- 1.5 GHz RT Oscilloscope has 233ps RT
- 2 GHz RT Oscilloscope has 175ps RT

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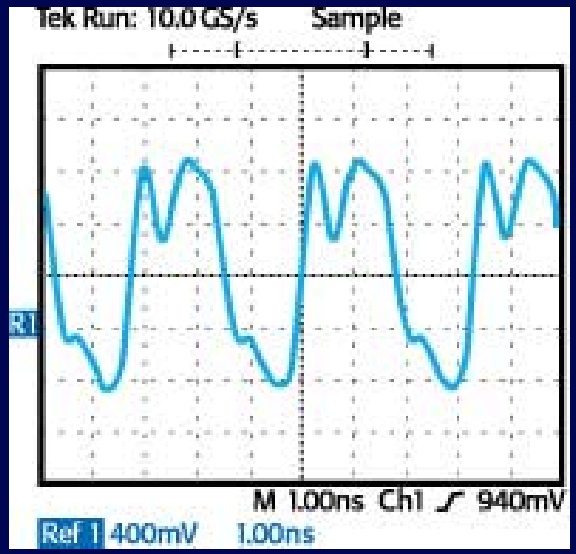
Rambus Rise/Fall Time Instrumentation Requirements

- Fast Signal Edges
- Pipeline Architecture
- Minimum Scope BW > 2 GHz
- Minimum Probe BW > 2GHz
- Minimum Scope SR > 8GS/s



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Rambus Rise/Fall Time Measurement Solutions

- **TDS694C Oscilloscope**
  - 3 GHz System Bandwidth at Probe Tip
  - 10 GS/s Sample Rate on Four Channels Simultaneously

- **P6249 Probe**
  - 4 GHz Active Probe
  - 20 k-Ohm impedance
  - 1 pf input capacitance
  - Small form factor

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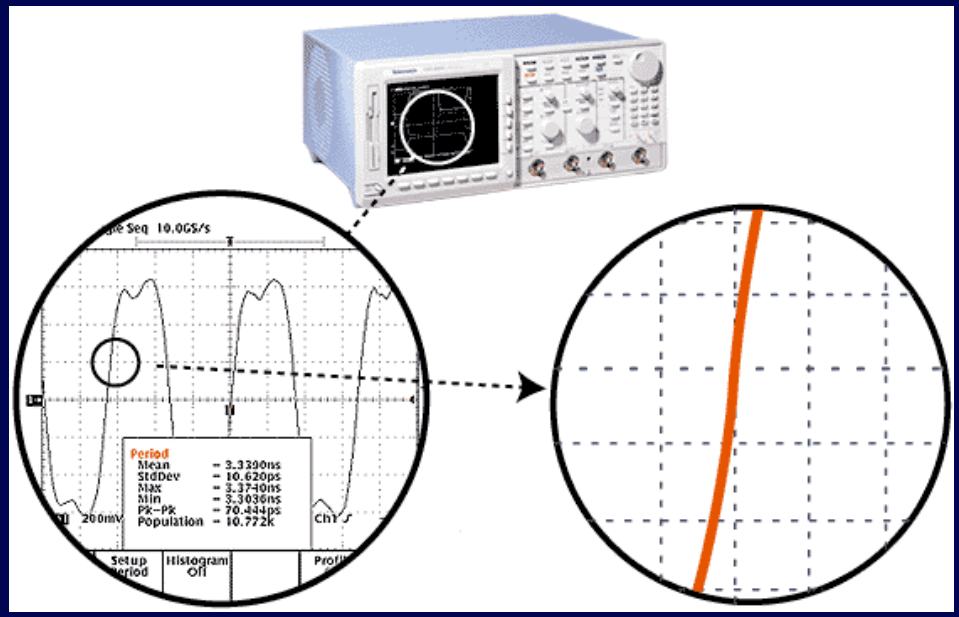
Rambus Technology Jitter Characterization Requirements

- Page 13, DRCG Data Sheet:

  Max Jitter = 100ps Peak-Peak

- Cycle-cycle Jitter Measurement
- Spread Spectrum Clocking



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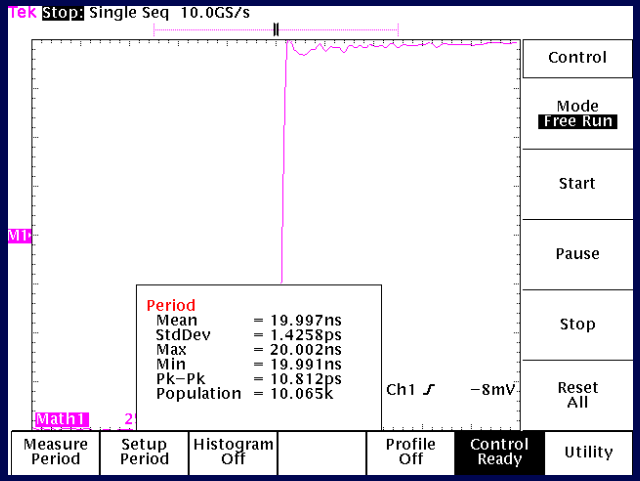
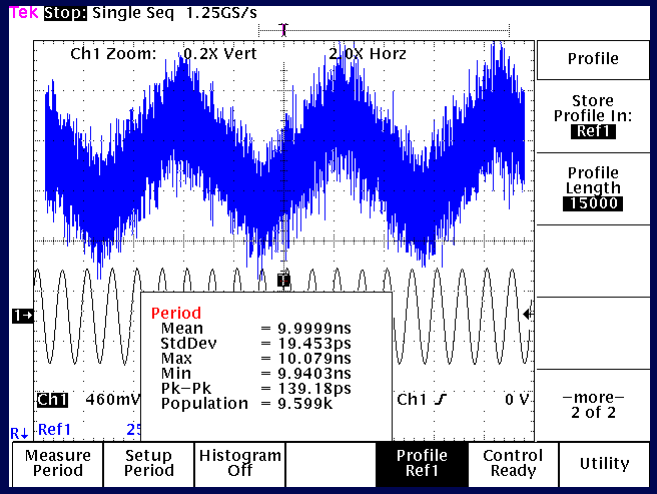
Rambus Jitter Instrumentation Requirements





- Low Jitter Signals
- Pipeline Architecture
- Timing Accuracy << 100ps
- Custom Timing Measurement Capabilities

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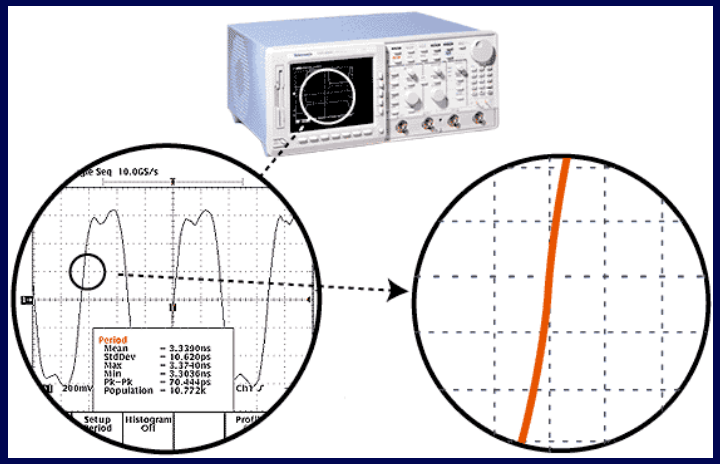
Rambus Jitter Measurement Solutions



- TDS694C 10GS/s, 3 GHz Oscilloscope
- TDSJIT1 <3ps RMS Jitter Measurement Application
- P6248 1.7 GHz Differential Probe
- DG2040 30ps Peak Jitter Signal Generator

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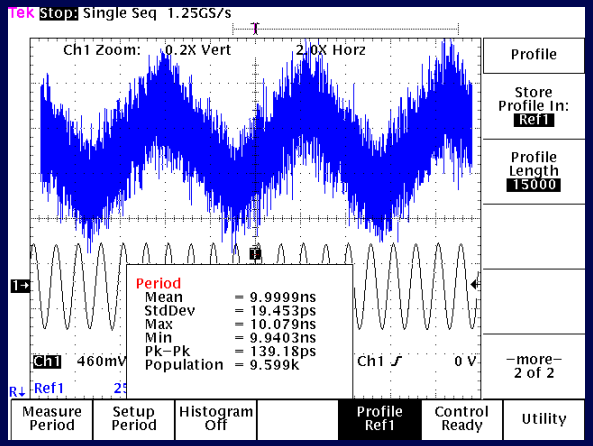
Jitter Measurements Available

- Comprehensive Histogram and Statistics
- Cycle-cycle Jitter Measurements
- N-Cycle Jitter Measurements
- Duty Cycle Measurements
- Spread Spectrum Clocking Analysis
- Analysis on 8M Record Lengths
- Jitter Profiling Feature



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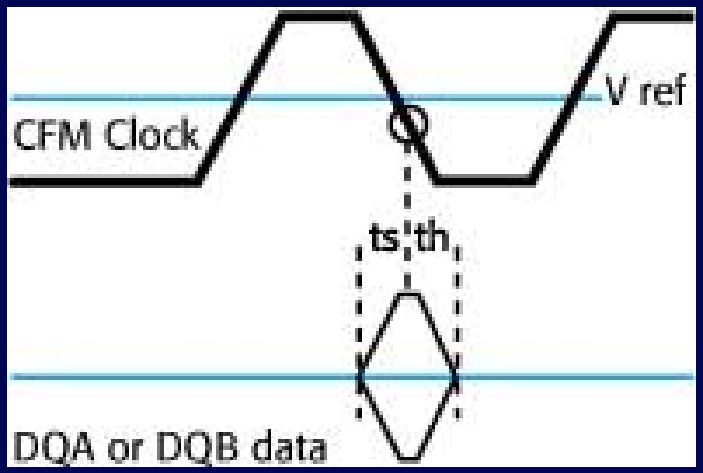
Rambus Technology Timing Characterization Needs

- **Page 34, Direct RAC Data Sheet:**

  Setup/Hold Timing = 200ps

- **Delay Timing**



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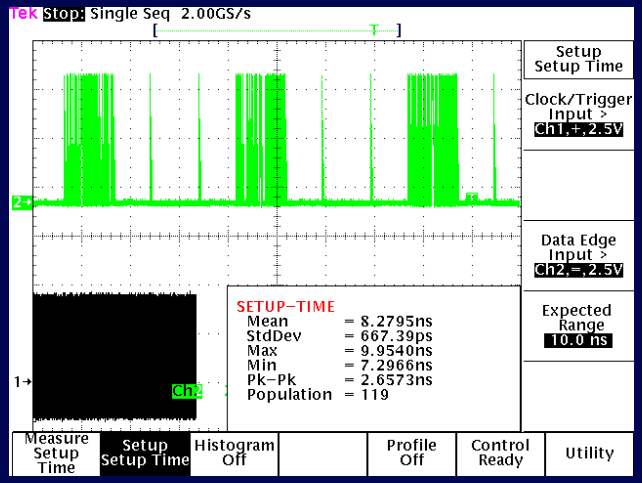
Rambus Timing Instrumentation Needs

- Stringent Timing Requirements
- Fast Signal Edges
- Pipeline Architecture
- Custom Timing Measurement Capabilities
- High SR, High BW Measurement
- Timing Accuracy <<200ps



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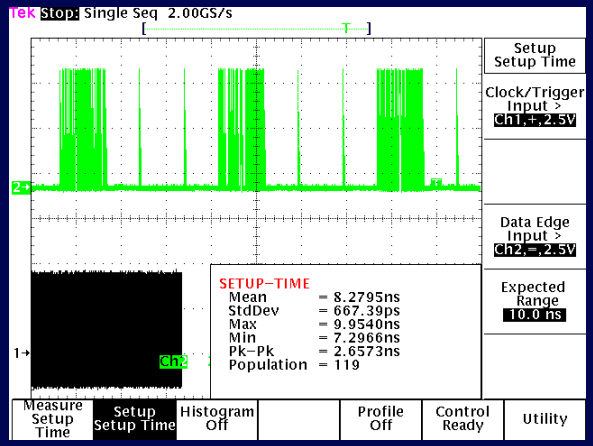
Rambus Timing Measurement Solutions

- TDS694C 10GS/s, 3 GHz Oscilloscope
- TDSPSM1 Timing Measurement Application
- P6249 4 GHz Active Probe
- P6248 1.7 GHz Differential Probe



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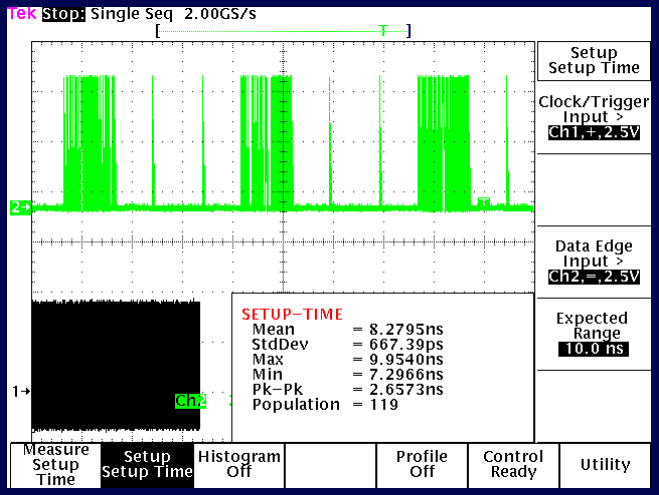
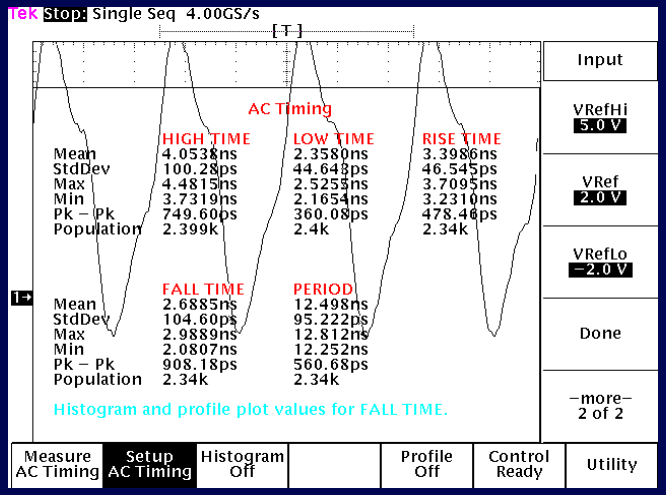
A Better Way to Make Timing Measurements





- Direct correlation of all timing measurements
- No approximations of set-up parameters
- Isolate negative or positive transitions
- Statistics, Histograms and Profile
- Multiple, single-shot AC Timing Measurements

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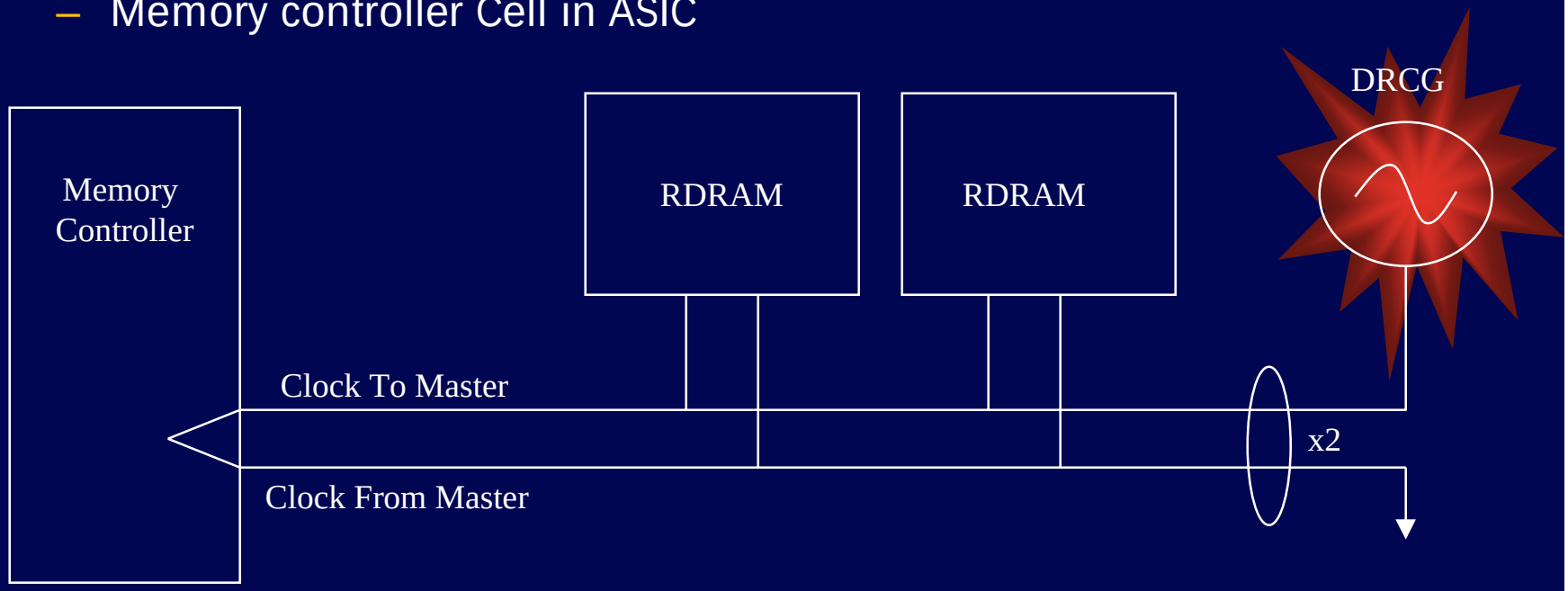
Rambus Clock Topology

- Pipeline architecture
- 800 M transfer rate
- Memory controller Cell in ASIC



Simplified Drawing of a Rambus Memory Subsystem Clock

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DRCG = Direct Rambus Clock Generator

Critical Rambus Clock Parameters

- DRCG “Direct Rambus Clock Generator”
  - IC Works
  - Cypress Semiconductor
  - Texas Instruments
  - Pericom

Check out the Rambus site for more information:

http://www.rambus.com

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Critical Rambus Clock Parameters

- Complementary outputs
- 400 MHz clock frequency
  - "double pumped" drives data at 800 Mbps
  - Driven through a resistor terminated transmission line
  - All high speed signals use low voltage 800 mV swing
- Clock generators are phase aligned with system clock to permit low latency and synchronization with system/core logic

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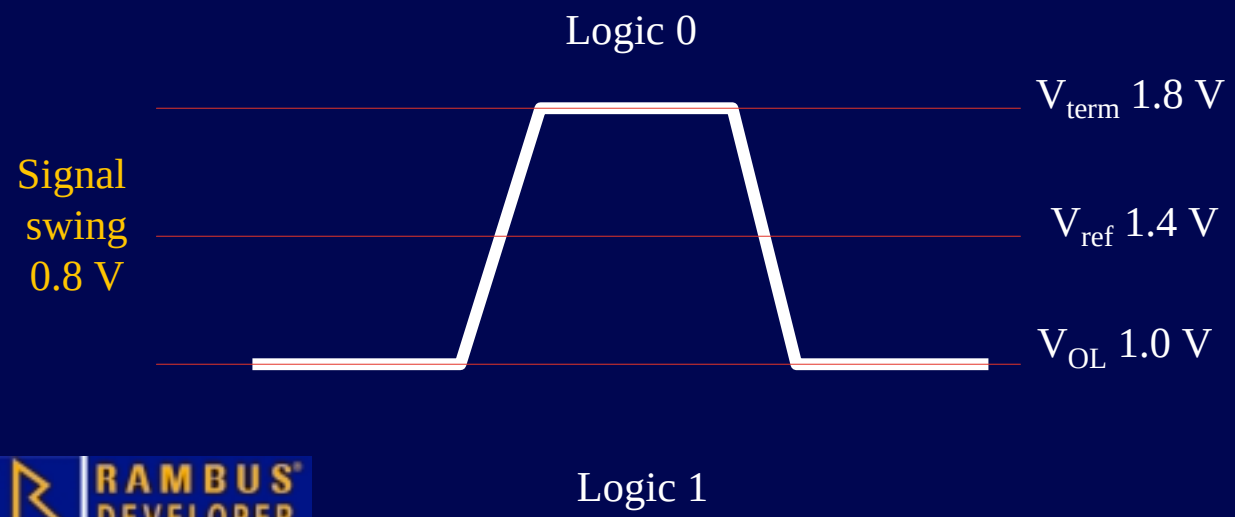
Critical Rambus Clock Parameters

- Gear logic used to “downshift” 800 MHz memory bus to slower system functions
- Some DRCG’s permit clock outputs to be tristated in test mode - useful for clock substitution



High-Speed signals use low voltage swings about V_{ref}.

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Critical Rambus Clock Parameters

- Typical DRCG Jitter specifications
  - Cycle to Cycle Jitter - 60 ps
  - Total Jitter over 2, 3, or 4 cycles - 100 ps
- 266 MHz Clock
  - Cycle to Cycle Jitter - 100 ps
  - Total Jitter over 2, 3, or 4 cycles - 160 ps

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Rambus Clock Substitution

- Clock Simulation
  - Dual Rambus channels
    - evaluate effects of switching noise & ground bounce
  - Jitter tolerance
    - manufacturing variability
  - Spread Spectrum Clocking
    - evaluate effects of spread spectrum clocks on EMI

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Rambus Clock Substitution

- Margin testing
  - debug Rambus systems with suspected jitter
  - vary amplitude symmetry
  - vary amplitude levels
  - vary duty cycle
  - vary clock skew in multi-channel Rambus implementations

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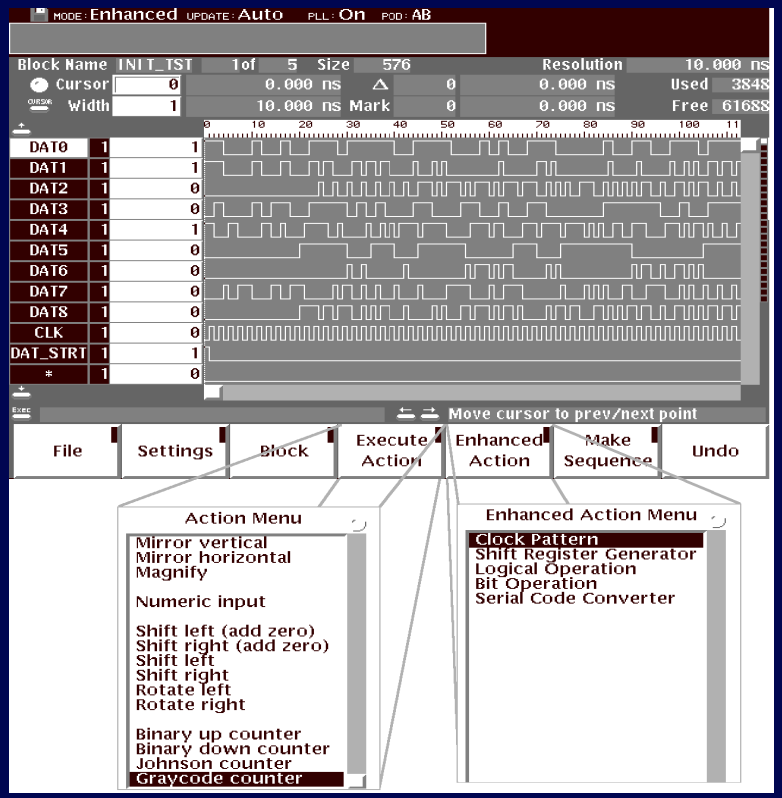
Rambus Clock Substitution Needs

- Max Jitter = 100ps Peak-Peak
- Cycle-cycle Jitter Measurement
- Spread Spectrum Clocking
- Setup/Hold Timing = 200ps
- Delay Timing



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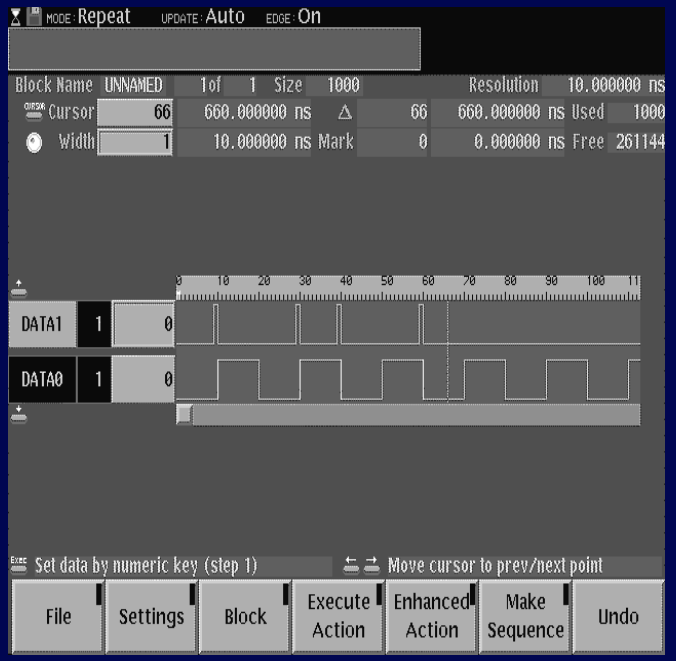
Rambus Clock Substitution Needs

- High Speed Bus
- Stringent Timing Requirements
- Fast Signal Edges
- Low Jitter Signals
- High Bit Rate Source
- Low Jitter Source



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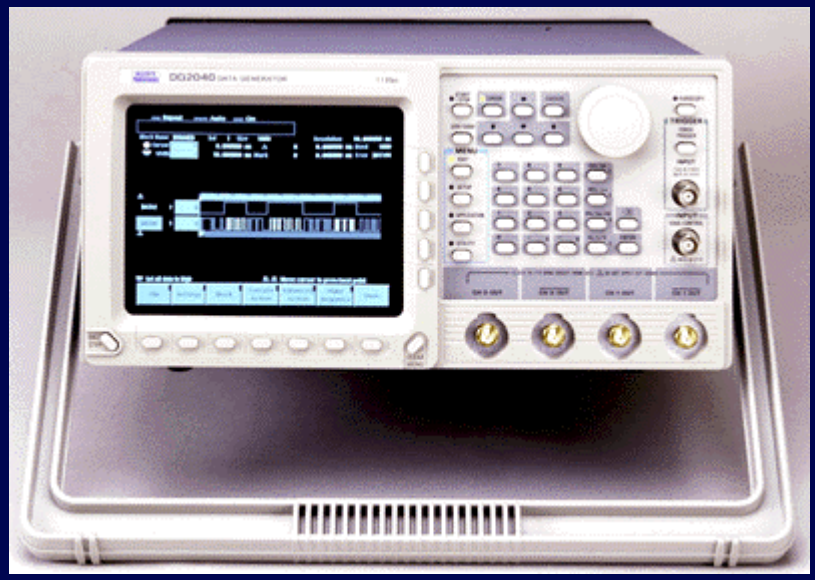
DG2040 - The Rambus Clock Debug Solution

- Key specifications
  - DC to 1.1 GHz
  - Programmable clock output on rear panel
    - Complementary outputs
    - Programmable amplitude
    - Programmable duty cycle
    - 25 mV to 2.5 V output swing



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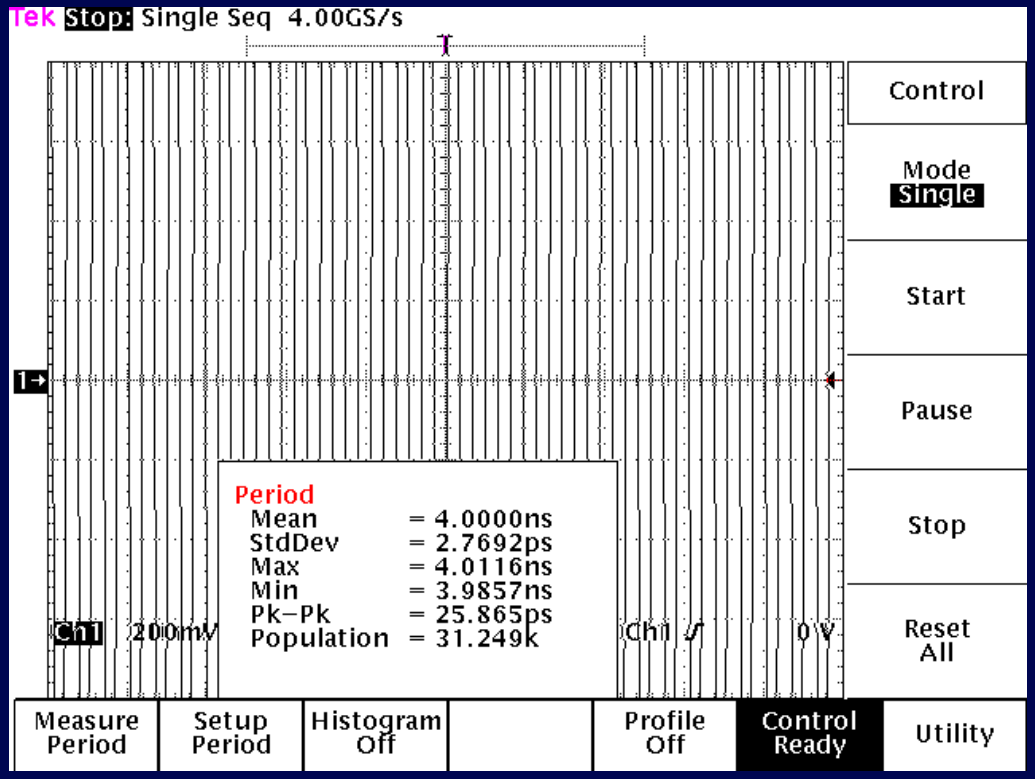
DG2040 - The Rambus Clock Debug Solution



Correct Setup of TDS 694C is crucial to showing the best results.

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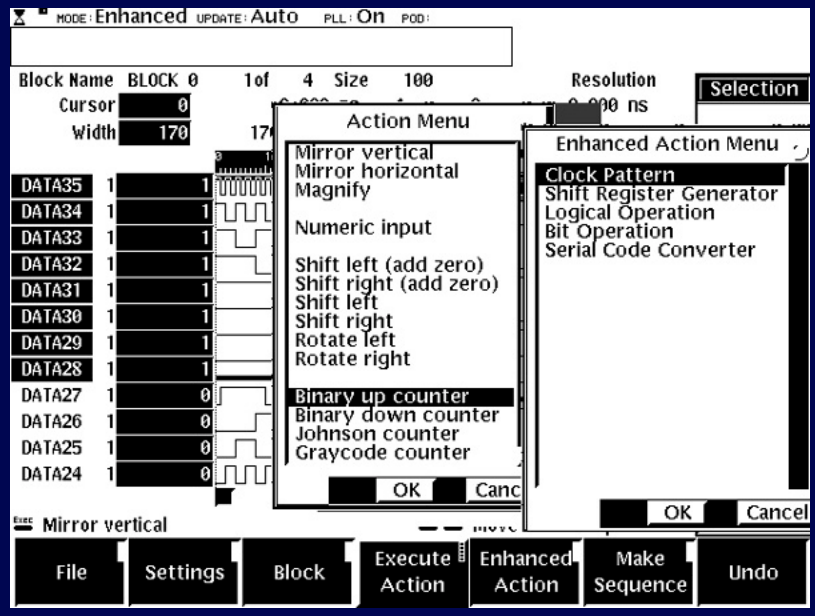
DG2040 - The Rambus Clock Debug Solution

- Data Output
  - Program data channels using “Enhanced Action” macro
  - Specify alternating 1s and 0s
  - Program amplitude
    - .25 mV to 2.5 V swing
  - Delay channel 0 to channel 1
    - inject skew



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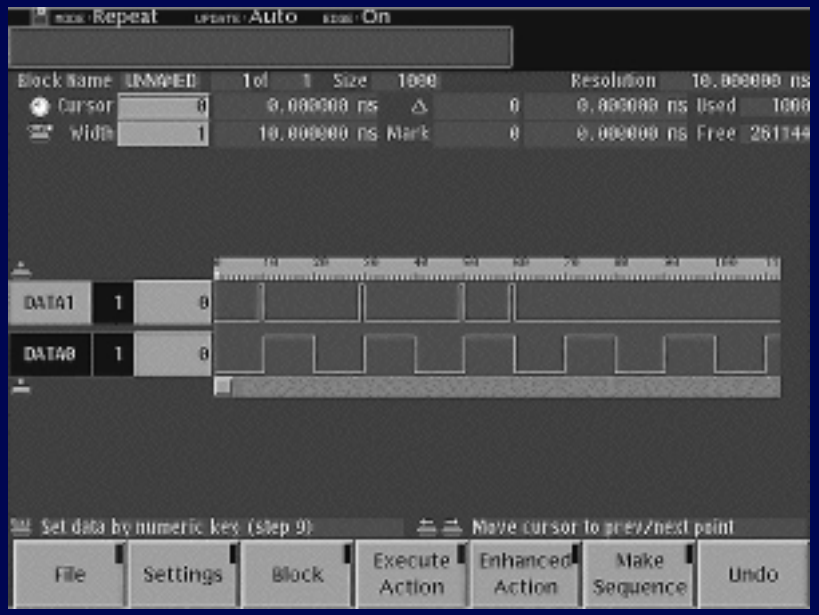
DG2040 - The Rambus Clock Debug Solution

- Edge Control - Evaluate Jitter Tolerance
  - Permits ultra fine control of delay of channel 0 to c.lock out
  - +/- 100 ps
  - Manual or external control
  - Add jitter with external modulation source
    - simulate power supply noise induced jitter



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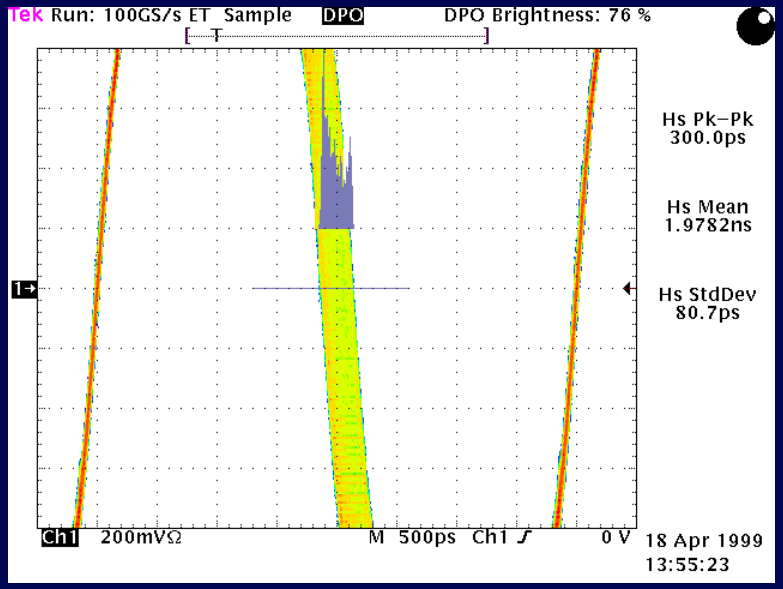
DG2040 Edge Control Example



- Jitter modulation signal is a 30 KHz sine, 2 Vpp, which is max edge control input
- DG was set up with mask data to enable all falling edges, triggered on rising edge
- Falling edge now has 300 pS pk-pk and 80 pS RMS jitter
  - Reducing the amplitude of the analog edge control signal produces less jitter
  - Changing the frequency and waveshape changes the time distribution of the jitter

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DG2040 - The Rambus Clock Debug Solution

- Key specifications
  - Jitter specifications
    - <30 ps pk to pk clock
    - <50 ps pk to pk data
  - Typical
    - <25 ps pk to pk clock
    - <30 ps pk to pk data
  - RMS <3 ps clock

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HFS9000

- For applications where multiple clocks are inserted in Rambus channel
- Need multiple 400 MHz outputs with skew control

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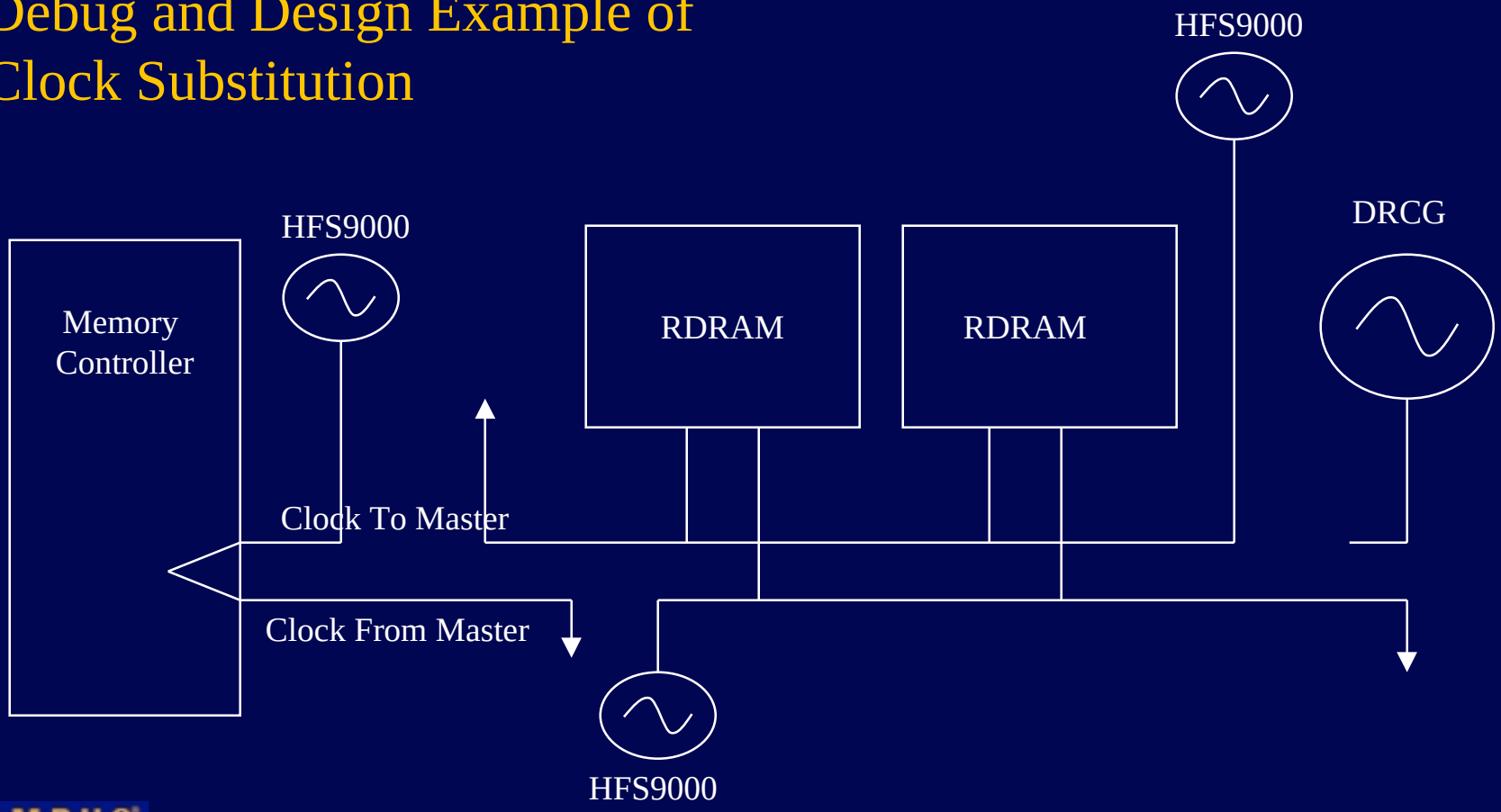
Rambus Practical Application

Debug and Design Example of Clock Substitution



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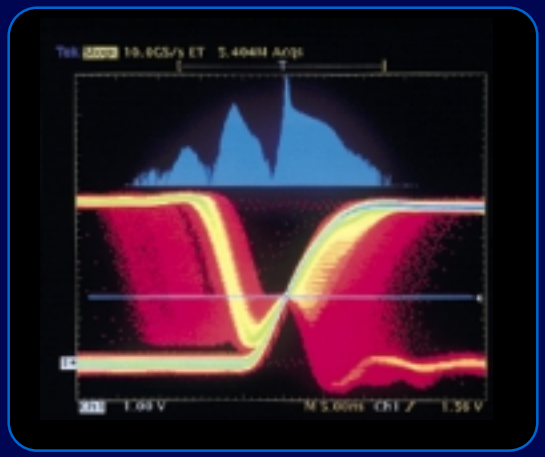
Rambus Glitch Detection



- **Digital Phosphor Oscilloscope**
  - **Detection and analysis of rare signal events**
  - **Fast waveform capture rate and frequency of occurrence information**

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Tektronix Signal Quality Solutions for Rambus

- TDS694C 10GS/s, 3 GHz Oscilloscope
- TDSJIT1 3ps RMS Jitter Measurement Application
- TDSPSM1 Timing Measurement Application
- TDS 794D Digital Phosphor Oscilloscope
- P6249 4 GHz Active Probe
- P6248 1.7 GHz Differential Probe
- DG2040 30ps Peak Jitter Signal Generator

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