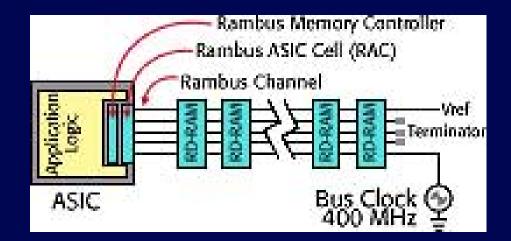
Rambus Signal Quality Measurements





Rambus Signal Quality Challenges



- High Speed Bus
- Stringent Timing Requirements
- Fast Signal Edges
- Low Jitter Signals
- Pipeline Architecture



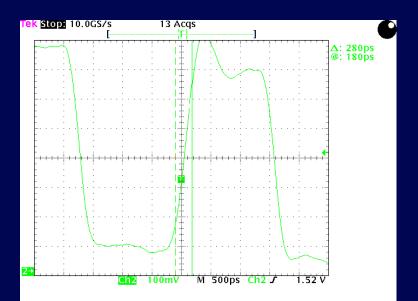


Rambus Technology Rise/Fall Time Requirements

Page 34, Direct RAC Data Sheet:

Rambus T_r and $T_f = 200$ ps

Source: www.rambus.com







Rambus Rise/Fall Time Instrumentation Requirements

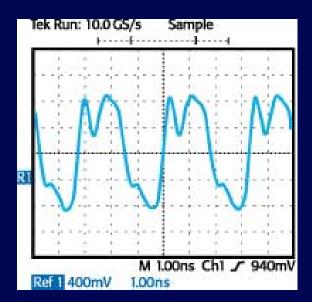
- 200ps RT Oscilloscope has BW = 0.35/T = 1.75GHz
- RT(measured) = SQRT[RT(oscilloscope)² + RT(probe)² + RT(Signal)²]
- RT (measured) = SQRT[200ps² + 200ps² + 200ps²] = 346ps!
- 1.5 GHz RT Oscilloscope has 233ps RT
- 2 GHz RT Oscilloscope has 175ps RT





Rambus Rise/Fall Time Instrumentation Requirements

- Fast Signal Edges
- Pipeline Architecture
- Minimum Scope BW > 2 GHz
- Minimum Probe BW > 2GHz
- Minimum Scope SR > 8GS/s







Rambus Rise/Fall Time Measurement Solutions

TDS694C Oscilloscope

- 3 GHz System Bandwidth at Probe Tip
- 10 GS/s Sample Rate on Four Channels Simultaneously
- P6249 Probe
 - 4 GHz Active Probe
 - 20 k-Ohm impedance
 - 1 pf input capacitance
 - Small form factor



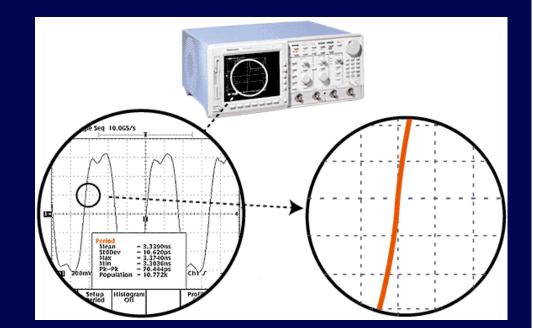






Rambus Technology Jitter Characterization Requirements

- Page 13, DRCG Data Sheet:
 - Max Jitter = 100ps Peak-Peak
- Cycle-cycle Jitter Measurement
- Spread Spectrum Clocking





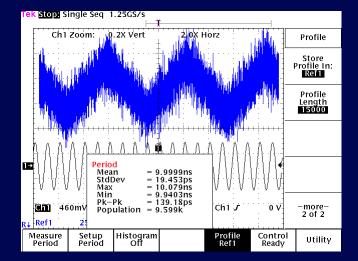


Rambus Jitter Instrumentation Requirements

Tek Stop: Single Seq 10.0CS/s									
-						Control			
						Mode Free Run			
5 5 6 6 7 7					- - 	Start			
M10 				-	- - - - - - - -	Pause			
	Max	n = 1 Dev = 1 = 2		- - - - 	Stop				
Math1		Pk = 1	9.991ns 0.812ps 0.065k	Ch1 J	-8mV	Reset All			
Measure Period	Setup Period	Histogram Off		Profile Off	Control Ready	Utility			

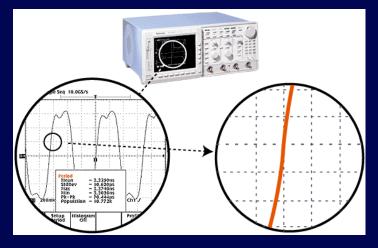
- Low Jitter Signals
- Pipeline Architecture
- Timing Accuracy << 100ps
- Custom Timing Measurement Capabilities







Rambus Jitter Measurement Solutions





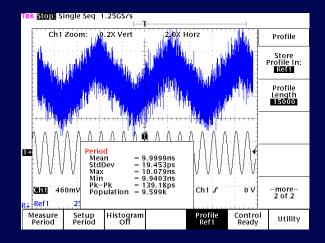
- TDS694C 10GS/s, 3 GHz Oscilloscope
- TDSJIT1 <3ps RMS Jitter Measurement Application
- P6248 1.7 GHz Differential Probe
- DG2040 30ps Peak Jitter Signal Generator





Jitter Measurements Available

- Comprehensive Histogram and Statistics
- Cycle-cycle Jitter Measurements
- N-Cycle Jitter Measurements
- Duty Cycle Measurements
- Spread Spectrum Clocking Analysis
- Analysis on 8M Record Lengths
- Jitter Profiling Feature

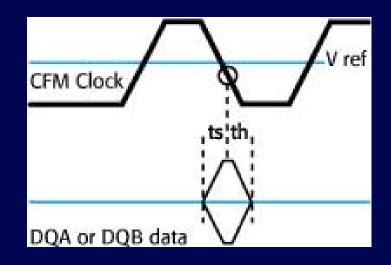






Rambus Technology Timing Characterization Needs

- Page 34, Direct RAC Data Sheet:
 Setup/Hold Timing = 200ps
- Delay Timing

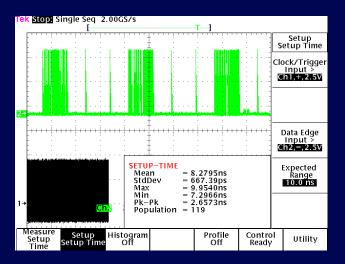






Rambus Timing Instrumentation Needs

- Stringent Timing Requirements
- Fast Signal Edges
- Pipeline Architecture
- Custom Timing Measurement Capabilities
- High SR, High BW Measurement
- Timing Accuracy <<200ps

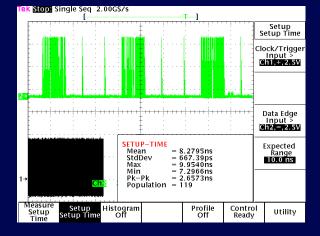






Rambus Timing Measurement Solutions

- TDS694C 10GS/s, 3 GHz Oscilloscope
- TDSPSM1 Timing Measurement Application
- P6249 4 GHz Active Probe
- P6248 1.7 GHz Differential Probe



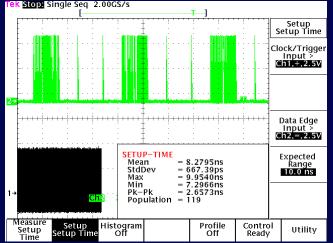


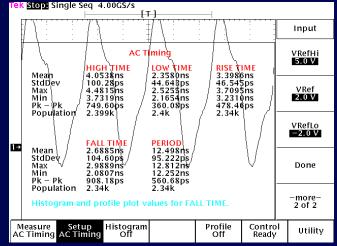






A Better Way to Make Timing Measurements





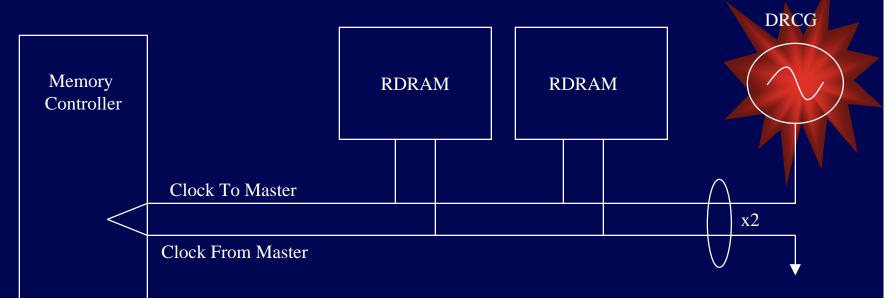
- Direct correlation of all timing measurements
- No approximations of set-up parameters
- Isolate negative or positive transitions
- Statistics, Histograms and Profile
- Multiple, single-shot AC Timing Measurements





Rambus Clock Topology

- Pipeline architecture
- 800 M transfer rate
- Memory controller Cell in ASIC



Simplified Drawing of a Rambus Memory Subsystem Clock **RAMBUS** DEVELOPER Tektronix

DRCG = Direct Rambus Clock Generator

- DRCG "Direct Rambus Clock Generator"
 - IC Works
 - Cypress Semiconductor
 - Texas Instruments
 - Pericom

Check out the Rambus site for more information:

http://www.rambus.com





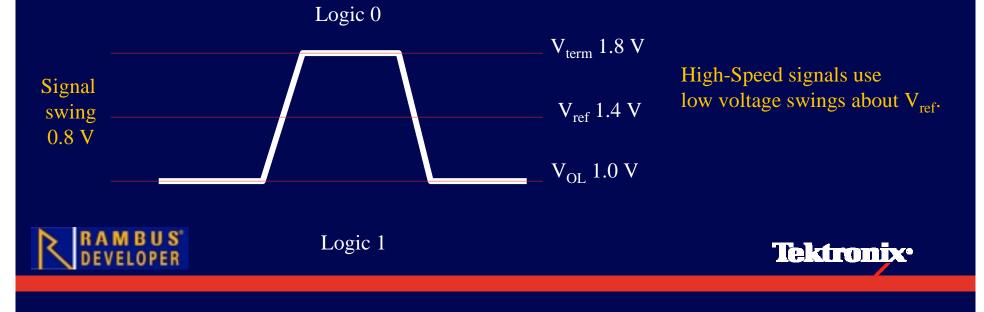


- Complementary outputs
- 400 MHz clock frequency
 - "double pumped" drives data at 800 Mbps
 - Driven through a resistor terminated transmission line
 - All high speed signals use low voltage 800 mV swing
- Clock generators are phase aligned with system clock to permit low latency and synchronization with system/core logic





- Gear logic used to "downshift" 800 MHz memory bus to slower system functions
- Some DRCG's permit clock outputs to be tristated in test mode - useful for clock substitution



- Typical DRCG Jitter specifications
 - Cycle to Cycle Jitter 60 ps
 - Total Jitter over 2, 3, or 4 cycles 100 ps
- 266 MHz Clock
 - Cycle to Cycle Jitter 100 ps
 - Total Jitter over 2, 3, or 4 cycles 160 ps





Rambus Clock Substitution

- Clock Simulation
 - Dual Rambus channels
 - evaluate effects of switching noise & ground bounce
 - Jitter tolerance
 - manufacturing variability
 - Spread Spectrum Clocking
 - evaluate effects of spread spectrum clocks on EMI





Rambus Clock Substitution

- Margin testing
 - debug Rambus systems with suspected jitter
 - vary amplitude symmetry
 - vary amplitude levels
 - vary duty cycle
 - vary clock skew in multi-channel Rambus implementations





Rambus Clock Substitution Needs

- Max Jitter = 100ps Peak-Peak
- Cycle-cycle Jitter
 Measurement
- Spread Spectrum Clocking
- Setup/Hold Timing = 200ps
- Delay Timing

MODE: Enh	nanced update: Auto PLL: On Pod: AB	;
Block Name	0 0.000 ns Δ	Resolution 10.000 ns 0 0.000 ns Used 3848
🛎 Width	1 10.000 ns Mark	0 0.000 пs Free 61688
<u> </u>		50 60 70 80 90 100 11
DATØ 1		
DAT1 1		
DAT2 1	00	
DAT3 1		
DAT4 1		
DAT5 1		
DAT6 1	QLL	
DAT7 1	<u>0</u> \\\\	
DAT8 1	<u>0</u>	
CLK 1	<u>0</u> ,000,000,000,000,000,000,000,000,000,	
DAT_STRT 1	1	
* 1	0	
–		
Exec		Move cursor to prev/next point
File	Settings Block Execute	Enhanced Make Undo
	Action Menu	Enhanced Action Menu
	Mirror horizontal Mirror horizontal Magnify Numeric input Shift left (add zero) Shift left Shift right (add zero) Shift left Rotate left Rotate left	Clock Pattern Shift Register Generator Logical Operation Bit Operation Serial Code Converter





Rambus Clock Substitution Needs

- High Speed Bus
- Stringent Timing Requirements
- Fast Signal Edges
- Low Jitter Signals
- High Bit Rate Source
- Low Jitter Source

X 💾 MODE : Re	peat u⊧	DATE: AUT	O EDGE : O	n			
Block Name	UNNAMED	1of	1 Size	1000		Resolution	10.000000 ns
🖀 Cursor	66	660.	000000 ns	Δ	66	660.000000	ns Used 1000
🕚 Width	1	10.	000000 ns	Mark	0	0.000000	ns Free 261144
÷		0 10	20 30		50 60		90 100 11
DATA1	0						
DATAO	0						
È							
🛎 Set data b	y numeric	key (step) 1)	<u> </u>	Move cur	sor to prev/n	ext point
File	Setting	js Bi	lock 📗	Execute Action	Enhanc Action		l Undo l



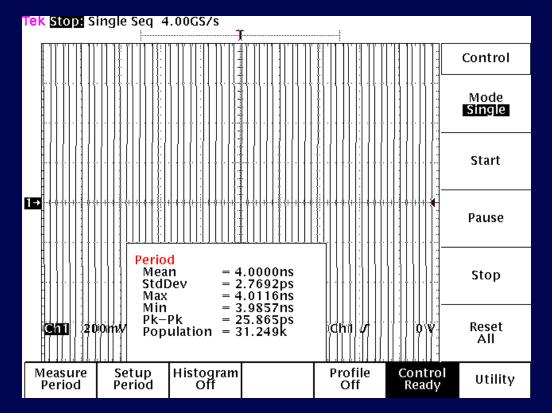


- Key specifications
 - DC to 1.1 GHz
 - Programmable clock output on rear panel
 - Complementary outputs
 - Programmable amplitude
 - Programmable duty cycle
 - 25 mV to 2.5 V output swing







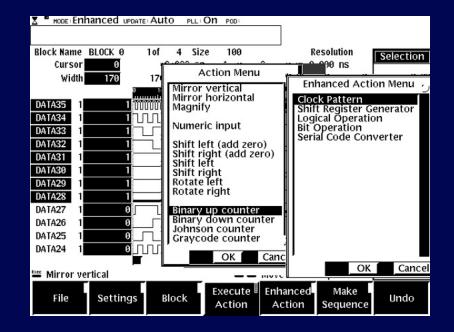


Correct Setup of TDS 694C is crucial to showing the best results.





- Data Output
 - Program data channels using "Enhanced Action" macro
 - Specify alternating 1s and 0s
 - Program amplitude
 - .25 mV to 2.5 V swing
 - Delay channel 0 to channel 1
 - inject skew







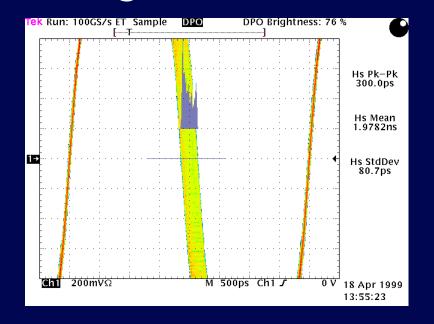
- Edge Control Evaluate Jitter Tolerance
 - Permits ultra fine control of delay of channel 0 to c.lock out
 - +/- 100 ps
 - Manual or external control
 - Add jitter with external modulation source
 - simulate power supply noise induced jitter

nas Ri	epeat .	etars: Auto	EDGE OF	1				
				2.52.75				
Block Name	UNAPED	10	1 Size	1000		Resolution		eeee ns
💮 Cursol			889968 ns	Δ	0	0.00000	ns Used	1008
🕿 Aida	1	10.0	00000 ns	Mark	0	0.000000	ns Free	261144
								-
÷				unut unut		al contraction of the		
DATA1	1	9						
DATAB	1							E.
and the second								
-				10000000000	Cale and the second		2266651	
the exercises	has not seen to	Loss Veters 1	0.		-	and to prove the	and an inter	
e sel data	by numeric	: key (step :		and in case of the local division of the	and an other designs of the local division o	sor to prev/n	Statement Street Street	
File	Settin	as Blo	ck I T		Enhance	the second second		ndo
				Action	Action	n Sequen	ice	





DG2040 Edge Control Example



- Jitter modulation signal is a 30 KHz sine, 2 Vpp, which is max edge control input
- DG was set up with mask data to enable all falling edges, triggered on rising edge
- Falling edge now has 300 pS pk-pk and 80 pS RMS jitter
 - Reducing the amplitude of the analog edge control signal produces less jitter
 - Changing the frequency and waveshape changes the time distribution of the jitter





- Key specifications
 - Jitter specifications
 - <30 ps pk to pk clock</p>
 - <50 ps pk to pk data</p>
 - Typical
 - <25 ps pk to pk clock</p>
 - <30 ps pk to pk data</p>
 - RMS <3 ps clock</p>







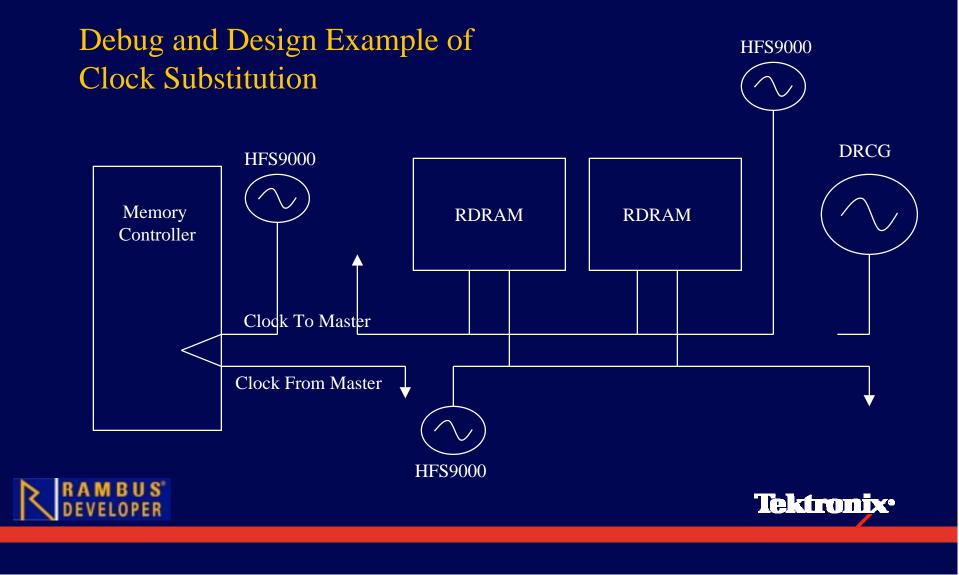


- For applications where multiple clocks are inserted in Rambus channel
- Need multiple 400 MHz outputs with skew control

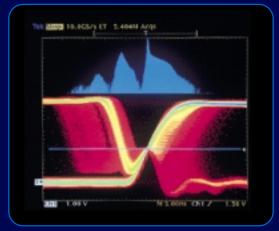




Rambus Practical Application



Rambus Glitch Detection



- Digital Phosphor Oscilloscope
 - Detection and analysis of rare signal events
 - Fast waveform capture rate and frequency of occurrence information





Tektronix Signal Quality Solutions for Rambus

- TDS694C 10GS/s, 3 GHz Oscilloscope
- TDSJIT1 3ps RMS Jitter Measurement Application
- TDSPSM1 Timing Measurement Application
- TDS 794D Digital Phosphor Oscilloscope
- P6249 4 GHz Active Probe
- P6248 1.7 GHz Differential Probe
- DG2040 30ps Peak Jitter Signal Generator



